A 22-mW 435-MHz DIFFERENTIAL CMOS HIGH-GAIN LNA FOR SUBSAMPLING RECEIVERS

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ABSTRACT

A low-power, high-gain CMOS low noise amplifier (LNA) for use as the first stage of a subsampling receiver is proposed. The performance of +96-dB voltage gain and less than 1-dB Noise Figure (NF) with very low power consumption is reported for the first time and makes it suitable for subsampling mixer with Track and Hold (T/H) circuit. The LNA contains both tuned and inductorless amplifier stages. The first stage utilizes optimum transistor gate width-length ratio (W/L), improved-Q on-chip spiral inductors, fully differential architecture, and current-reuse technique to achieve low-noise, high-gain, and low-power at the same time. The following stages are inductorless amplifiers designed to achieve the maximum-gain. Cascode transistors are used in all stages to maintain reasonable gain at high frequencies and to achieve good reverse isolation. The amplifier linearity is sacrificed as a consequence of its high gain.

1. INTRODUCTION

Low power consumption is always the first priority for deep-space communications. The power consumption governing a digital CMOS based system is $P \propto CV^2f$ where $C$ is the capacitance in the circuit, $V$ is the supply voltage, and $f$ is the clock speed [1]. Unlike the traditional mixer whose local oscillator works at the RF frequency, subsampling architecture operates at a very low frequency with potential to achieve low-power consumption. Fig. 1 shows a basic subsampling receiver block diagram.

The subsampling mixer is indeed a T/H circuit. The required milli-volts input level and inherently high NF (~20-30dB) makes it necessary to use a low-noise, high-gain LNA prior to it. Most authors went after expensive BiCMOS process [2], while others sacrificed noise with power [3]. With innovations in architectures, this paper demonstrates the possibility to achieve low-power and high-gain LNA with standard CMOS process.

In order to achieve low noise figure, the first stage adopts several design practices: 1) optimum transistor gate $W/L$ for low-noise, 2) inductive source degeneration for 50Ω input impedance, 3) fully-differential topology for substrate noise rejection, and 4) dual-layer spiral inductors for high-$Q$. Both on-chip and off-chip inductors are used to match the input impedance at the operating frequency. With current-reuse technique, first stage LNA is able to provide 30dB gain with 10.2mW power consumption.

The following stages are designed to achieve reasonable voltage gain using inductorless LNA. Four stages are cascaded, each with 12-dB gain and 2.78-mW power consumption, to achieve ~50dB-gain.

2. FIRST STAGE ARCHITECTURE

Low noise figure (NF), gain, and the input matching are achieved in the first stage of the high-gain LNA.

2.1. Noise optimization

The overall noise factor ($F$) of an $N$-stage series connected system is [4]

$$F = F_1 + \frac{F_2 - 1}{A_1 A_2} + \ldots + \frac{F_N - 1}{A_1 A_2 \ldots A_{N-1}}$$

where $F_i$ and $A_i$ are noise factor and gain of each stage, respectively. The noise in the first stage is carried over throughout the entire system without any reduction.

For a given power consumption, the optimum CMOS transistor gate width, $W_{opt}$, for minimal noise figure can be approximated by [5],

$$W_{opt} \approx \frac{1}{3\omega L_{gate} C_{ox} R_{IN}}$$

where $\omega$ is the operation frequency (in rad.), $C_{ox}$ is the oxide capacitance per unit area, $R_{IN}=50\Omega$ is the input impedance, and the $L_{gate}$ is the effective gate length. In order to keep the transistor working at high frequency (to keep $f_T$ high), the transistor gate length $L$ is chosen to be the minimum length allowed by the process.

For better noise performance and input impedance-matching purposes, inductive source degeneration architecture is used in the first stage of LNA (Fig. 2). The source inductance $L_S$ is chosen to make the real part of the gate impedance equal to the antenna impedance (50Ω in our case); the off-chip tuning gate inductor $L_G$ is to cancel the imaginary part of the input impedance. The real and imaginary parts of the impedance at the gate are given as following:
In order to increase the quality factor \( Q \) of the on-chip spiral inductors \( \text{LS} \) and \( \text{LD} \), they are realized using dual metal layers (metal3 and metal2). Physical model [6] serves as initial design and then verified with Fast Henry CAD tool provided by Cadence. For small realization, \( \text{LS} \) is chosen to be 2302 \( \mu \)m while \( \text{LD} \) is limited to be 500 \( \mu \)m. As a consequence, transistor sizes need to be adjusted to tune to the operating frequency. \( \text{LG} \) are commercially available off-chip surface mount (SM) inductors.

2.2. Current-reuse technique

In order to leave more room for the second stage, 2.5-V supply voltage is used for all stages. With such high voltage, it allows us to stack another LNA on top of the input stage. The output (drain of \( M_2 \)) of the input stage is coupled to the input (gate of \( M_3 \)) of the top stage through a coupling capacitor \( C_p \). The top stage is like a replica of the input stage. However the input impedance is no longer important because the voltage gain, instead of the power gain, is of our interest now. The gate inductors are therefore exempted from this stage. The load inductors \( L_L \) are chosen to be 560 \( \mu \)m due to area limitation. Current-reuse technique is employed so that both LNAs share the same dc bias current (Fig. 2).

The LNA is designed to be fully-differential in order to suppress substrate noise that appears as a common-mode signal.

When terminated to the input of the second stage LNA, the first stage LNA provides 48.65-dB voltage gain, 0.85-dB \( NF \), -43.7dB \( S_{11} \), and 30.15dB \( S_{21} \) with power consumption at 10.2mW. Table II and Fig. 5 summarize the simulation results.

3. SECOND STAGE ARCHITECTURE

Voltage gain is the main concern for the follow stages of the LNA. Inductorless topology is required to reduce the layout size. Multi stages are needed to achieve milli-volts peak-to-peak output level for the T/H circuit.

3.1. Cascoded topology with resistive loads

Active inductor LNA is a popular candidate [7], but it is power hungry, high noise, prone to oscillate, and may cause gain ripple when combined with the first stage LNA. Push-pull amplifier shows very good gain and power, however, is difficult to bias precisely. Cascoded LNA is the remaining option for high-gain, low-power at high-frequency applications. Active load, due to parasitic capacitance, fail to respond well at our frequency of interest. After extensive considerations of different topologies, cascoded LNA with resistive load is chosen for its easy feasibility, high-gain, low-power, and low-noise.

3.2. Gain maximization

The small-signal voltage gain of the cascoded LNA shown in Fig.3 is

\[
A_p = \frac{g_{m3} + g_{m2} + g_{mnh2}}{g_{m1} + g_{m2} + g_{mnh2}} \approx g_{m1} R \quad (1)
\]

As a start, it seems possible to have high gain if \( R \) is very large. However, this contradicts with the low-power requirements that one needs to use reduced supply voltage.

Recall for the long channel device,

\[
I_D = \frac{\mu_n C_{ov} W}{2} \left( V_{gs} - V_t \right)^2 \left( 1 + AV_{DS} \right) \quad (2)
\]

\[
g_m = \frac{\mu_n C_{ov} W}{L} \left( V_{gs} - V_t \right) \left( 1 + AV_{DS} \right) = \frac{2I_D}{V_{gs} - V_t} \quad (3)
\]

\[
g_{mnh} = \frac{g_m}{2\sqrt{\phi - V_{dso}}} \quad (4)
\]

\[
g_{ds} = \frac{I_D}{V_{ds}} \quad (5)
\]

and

\[
R = \frac{V_{DD} - V_{dso} - V_{dso2}}{I_D} \quad (6)
\]
Substituting equations 2 and 3 into equation 1 yields:

\[
A_y = \frac{1}{1 + \frac{r_{ds2}}{g_{m2} + g_{mb2}} + \frac{2}{1 + 2(\phi + \frac{V_{gs2}}{V_{th2}})^2 \frac{1}{2}\frac{1}{V_{GS1}} - \frac{1}{V_{GS2}}}}
\]

(4)

If the overdrive voltages \(V_{od1} = (V_{GS1}-V_{th1})\) and \(V_{od2} = (V_{GS2}-V_{th2})\) are given, the voltage gain becomes dependent only on \(V_{DS1}\) and \(V_{DS2}\). The derivation to find the exact solution would be tedious. Using computer program to find the optimum values numerically is more convenient. Fig. 3c shows the voltage gain verses \(V_{DS1}\) and \(V_{DS2}\) in 3-D and 2-D plots for \(V_{DD} = 2.5\) V and \(V_{DS1} = V_{DS2} = 0.2\) V. In fact, once the overdrive voltages are given, the maximum gain is fixed. The corresponding \(V_{DS1}, V_{DS2}, V_{G1},\) and \(V_{G2}\) are also fixed. For a given \(I_{DS}\), \(R\) is determined from equation 3. The resulting \((W/L)_1\) and \((W/L)_2\) are determined using equation 2.

The high-gain can be achieved using high \(V_{DD}\) or low overdrive voltages. However, the major difficulties are: 1) as mentioned before, we really don’t have much room to play with \(V_{DD}\) and it is set to be 2.5-V at last; 2) very low-overdrives are not practical because very wide transistors are needed; and 3) performance of low-overdrive designs is subject to the accuracy of the quiescent points, of which may be difficult to keep, especially when the output swing is high. On the other hand, although the small signal model is for ac, it does not include any frequency dependent variables. One may come up with an extremely high-gain design only to realize it works for dc or very low frequencies.

### 3.3. Cascaded multi stages

In order to achieve high-gain, more than one stage inductorless LNAs are needed. As a start, with limited power budget, 12-dB gain on each inductorless stage is targeted. In order to reach the voltage level that is able to drive T/H circuit, four inductorless stages in series are proposed.

### 4. OVERALL PERFORMANCE

**Cadence Spectre** simulations show the overall voltage gain to be 64.789 in magnitude (+96.23dB), \(S_{11}\) of +77.04dB, \(S_{11}\) of -43.1dB, \(NF\) of +0.86dB, and \(P_{d}\) of 22mW.

The subsampling receiver architecture requires amplifying the input signal (~130 to ~90dBm, or 0.1 to 10\(\mu\)V_{pp}) [8] from antenna to several milli-volts that T/H circuit can detect. If an amplifier is to work linearly throughout the specified range, then with 0.1\(\mu\)V_{pp} input it has 1mV_{pp} output, and with 10\(\mu\)V_{pp} input it will have 100mV_{pp} output, which is no longer a small signal but is comparable to the bias voltages and can change the quiescent points of the later stages. The overall performances are shown in Fig. 6 and Table III. Detailed post-layout parasitic effects are not considered at this time.

### 5. CONCLUSIONS

A multi-stage high-gain LNA with relatively low power consumption has been designed. The amplifier is designed to meet the specifications of a RF front-end for subsampling receiver for deep-space applications. The LNA trades off linearity for the required high voltage gain. The very high-gain comes from the stages, in which series of four gain-optimized cascaded inductorless LNA are connected. The overall low noise figure of the LNA is due to optimum design of the first stage. Current-reuse technique is employed in the first stage for low-power design. The novel architecture brought overall high-gain, low-power, and low-noise that outperformed state-of-the-art designs.
Low power consumption makes direct RF subsampling receiver architecture a promising choice for deep space communication. The high-gain LNA designed in this work may find other uses.

The high-gain LNA is implemented in HP-Agilent process. Active die area of the LNA is 1.3mm × 1.8mm.

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7. REFERENCES


